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## REMARKS/ARGUMENTS

Favorable reconsideration of this application, as amended, is respectfully requested.

Without intending to limit the scope of Applicants' claims, Applicants are presenting the following remarks to assist in a general understanding of the invention.

### Applicants' Invention

Characteristics of the invention of this application are: (1) since an insulating film is formed on a MISFET by high-density plasma CVD at a temperature of 450° to 700°C, it is possible to form an insulating film with small moisture and impurity content; and (2) after trenches are formed in the insulating film formed by high-density plasma CVD and a silicon film is deposited on the insulating film and in the trenches, the silicon film on the insulating film is removed, and then, HSG is selectively formed only on the silicon film in the trenches, thereby forming lower electrodes only on the inner surfaces of the trenches. By performing the process of depositing a high-density plasma CVD film on the portion where the capacitor is to be formed, by forming the trenches in this high-density plasma CVD film, and by forming the lower electrodes of capacitors

in the trenches, the lower electrodes of the capacitors can be formed with good HSG not influenced by degassing (see Applicants' specification, p.4, line 24 to p.5 line 5, and p.18, line 13 to p.19 line 2).

Differences Between the invention and Tsai (5,763,306)

In Tsai, polysilicon 19 is formed in the trenches formed in an insulating film and on the insulating film, and in this condition, HSG 20 is formed. Thereafter, polysilicon and the HSG on the insulating film are removed to form the lower electrodes in the trenches (Figs. 8A, 8B, and 9A). In this case, the growth of the HSG is hindered by degassing from the insulating film, pointed out as a problem in this application, and it is impossible to form good HSG. In the invention, after silicon is deposited in trenches formed in an insulating film and on the insulating film, and the silicon on the insulating film is removed, the silicon (43a) is left only in the trenches, and then, HSG (43b) is selectively grown only on the silicon in the trenches.

More specifically, in Tsai, the inside and outside of the trenches are covered with the polysilicon 19, and no consideration is given to degassing from the SiN film 13 at

the time of forming the HSG 20. There is no teaching or suggestion in Tsai that an insulating film is formed by high-density plasma CVD so as to eliminate the influence of degassing. In the invention, the HSG is selectively formed only on the silicon in the trenches, and it is essential that the insulating film be formed by high-density plasma CVD (see p.18, line 13 to p.20, line 3).

Differences between the invention and Basceri et al. (6,589,839)

In FIG. 1 of Basceri, the insulating film 22 is formed of BPSG and the lower electrode of the capacitor 26 is formed in the trenches and on the insulating film 22. Then, the lower electrode 26 on the insulating film is removed by a planarization process (col.5, line 50 to col. 6, line 7). Doped polysilicon and HSG are disclosed as the lower electrode (col.6, lines 8 to 23) . The HSG 28 is formed on the polysilicon 26 formed in the trenches in the insulating film and the HSG is formed by gas phase nucleation or surface seeding (col.8, lines 14 to 20). However, only BPSG is disclosed as the insulating film in which the trenches are formed in Figs. 1 and 4.

If the trenches are formed in the BPSG using the BPSG as the insulating film, and the HSG on polysilicon for the lower electrode of the capacitor is formed as described above, the formation of the HSG is hindered by degassing from the BPSG. There is no disclosure of this problem in Basceri. Furthermore, the lower electrode 26 is left in the trenches by using the planarization method. In the invention, after coating photoresist in the trenches, the polysilicon on the insulating film is removed by etching back, and the polysilicon in the trenches is not removed.

In the rejection of Applicants' claims, it is stated that it is known in the semiconductor art to deposit an insulating layer by using high-density plasma CVD and that it would have been obvious to a person of ordinary skill to deposit an insulating layer using high-density plasma CVD in Tsai. However, high-density plasma CVD is conventionally used only to form an interlayer insulating film between multi-layered wirings and to fill wiring portions. This is because high-density plasma CVD is effective to achieve flatness when filling a narrow space. Also, apparatus for forming a high-density plasma CVD film is expensive and is usually used to fill an uneven space. In Basceri and in Tsai, there is no disclosure, as in this

application, that an insulating film is formed on a flat portion by using high-density plasma CVD and in trenches formed in an insulating film. In this application, high-density plasma CVD is not used to fill an uneven space, but is used to reduce degassinq from the insulating film. Deposition of an insulating film on a flat portion by the use of expensive high-density plasma CVD would not be suggested to those having standard knowledge. In ordinary cases, BPSG or a standard plasma CVD film might be used for the deposition of an insulating film on a flat portion, but in Applicants' invention, a high-density plasma CVD film is deposited on a flat portion.

Turning to the claims, independent Claim 1 has been amended to recite "forming an insulating film above said MISFET by a high-density plasma CVD method at a temperature of 450°C to 700°C" and to recite "depositing a silicon film on said insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said insulating film and removing the silicon film from said insulating film to leave the silicon film only on an inner surface of said trench".

Independent Claim 6 has been amended to recite "depositing a second insulating film on said first

insulating film at a second temperature between 450°C and 700°C that is higher than said first temperature by a high-density plasma CVD method" and "depositing a silicon film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench".

Independent Claim 11 has been amended to recite "forming a plug connected with said MISFET through a first insulating film which has a substantially planarized surface"; "forming a second insulating film containing impurity over said first insulating film by a high-density plasma CVD method at a temperature of 450°C to 700°C"; "forming a trench by etching said second insulating film"; "depositing a second film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench"; "forming a rugged surface silicon film on said silicon film to form a lower electrode of a capacitor on the inner wall of the trench"; and

"forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film".

Independent Claim 14 has been amended to recite "forming a second insulating film containing impurity on said first insulating film at a second temperature higher than said first temperature by a high-density plasma CVD method" and "depositing a silicon film on said second insulating film and in said trench, filling said trench by a photoresist, then etching back said silicon film on said second insulating film, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench.

It will be apparent from the foregoing comments regarding the invention and the prior art, that the additional features now recited in the independent claims distinguish patentably from the prior art, even if the references are combined in the manner proposed in the rejection under 35 U.S.C. § 103(a). The rejection recognizes that Tsai, the principal reference, does not teach removing the silicon film on the second insulating film to leave the silicon film only on an inner surface of the trench, and depositing an insulating layer by using

high-density plasma CVD. The rejection proposes to cure this deficiency of Tsai by reliance upon Basceri et al. However, as pointed out in the foregoing comments, there is no teaching or suggestion in Basceri et al. (or in Tsai) of using high-density plasma CVD in an environment such as that recited in Applicants' claims. In other words, there is no suggestion in the prior art of combining the teachings of the references in any manner that could reasonably be expected to produce the inventions recited in Applicants' claims.

Accordingly, it is respectfully submitted that all of the claims now presented should be allowed and that this application should be passed to issue.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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